IN THE CLAIMS

Please cancel claims 9-17 and amend claim 1 as follows all without prejudice.

1. (Currently amended) A semiconductor device structure, comprising:

a PMOS device ~~200~~ and an NMOS device ~~300~~ disposed on a substrate ~~1,2~~,

the PMOS device ~~200~~ including a compressive layer [[~~6~~]] stressing an active region [[~~3~~]] of the PMOS device,

the NMOS device ~~300~~ including a tensile layer [[~~9~~]] stressing an active region [[~~3~~]] of the NMOS device, wherein

the compressive layer includes a first dielectric material [[~~6~~]], the tensile layer includes a second dielectric material [[~~9~~]], and the PMOS and NMOS devices are FinFET devices ~~200,300~~.

2. (Original) The semiconductor device as claimed in claim 1, wherein the first dielectric material comprises SiN.

3. (Original) The semiconductor device as claimed in claim 1, wherein the second dielectric material comprises SiN.

4. (Original) The semiconductor device structure as claimed in claim 1, wherein the first dielectric material has a substantially uniform compressive stress in a range of -300 MPa to -3000 MPa.

5. (Original) The semiconductor device structure as claimed in claim 1, wherein the first dielectric material has a substantially uniform thickness in a range of 200Å to 2000Å.

6. (Original) The semiconductor device structure as claimed in claim 1, wherein the second dielectric material has a substantially uniform tensile stress in a range of +200 MPa to +2000 MPa.

7. (Original) The semiconductor device structure as claimed in claim 1, wherein the second dielectric material has a substantially uniform thickness in a range of 200Å to 2000Å.

8. (Original) The semiconductor device structure as claimed in claim 1, wherein the first dielectric material and the second dielectric material are SiN.

9. (Cancelled) A method for manufacturing a semiconductor device structure, comprising:

providing a p-FinFET device region **200** and an n-FinFET device region **300** on a same substrate **1,2**;

disposing a first liner **5** on the p-FinFET device region and the n-FinFET device region;

disposing a compressive film **6** on the first liner;

disposing a first mask **7** on the p-FinFET device region;

removing the compressive film from the n-FinFET device region;

removing the first mask **7**;

disposing a second liner **8** on the p-FinFET device region and the n-FinFET device region;

disposing a tensile film **9** on the second liner;

disposing a second mask **10** on the n-FinFET device region;

removing the tensile film from the p-FinFET device region; and

then removing the second mask.

10. (Cancelled) The method as claimed in claim 9, wherein said step of disposing a compressive film includes depositing a compressive film having a film stress of about -1400 MPa.

11. (Cancelled) The method as claimed in claim 9, wherein said step of disposing a tensile film includes depositing a tensile film having a film stress of about +500 MPa.

12. (Cancelled) The method as claimed in claim 9, wherein the compressive film is SiN.

13. (Cancelled) The method as claimed in claim 9, wherein the tensile film is SiN.

14. (Cancelled) The method as claimed in claim 9, wherein the compressive film is disposed having a substantially uniform thickness in a range of 200Å to 2000Å.

15. (Cancelled) The method as claimed in claim 9, wherein the tensile film is disposed having a substantially uniform thickness in a range of 200Å to 2000Å.

16. (Cancelled) The method as claimed in claim 9, wherein said step of disposing a compressive film includes depositing a compressive film having a film stress of greater than about -1400 MPa.

17. (Cancelled) The method as claimed in claim 9, wherein said step of disposing a tensile film includes depositing a tensile film having a film stress of greater than about +500 MPa.